

Exercise 1

Design an L1 cache (number of bits for tag, entry, ...) for a CPU with 32-bit address in 3 following types. The cache size is 32KB, block (line) size is 32 byte

- Direct mapped
- Fully Associative
- 4 way associative



Exercise 2

For the cache in Exercise 1, assumed the cache is 4-way associative, how many cache hit, miss occur if the CPU execute the following memory access sequence in case of

- Write through no write allocation
- Write back with write allocation

RD 0x00000000, WR 0x01000000, RD
0x01000010, WR 0x02000050, RD 0x02000058



Exercise 3

How much faster/slower is a unified 32KB cache than a separated 16KB I/16KB D cache if the miss rate is ones in the following slide table, and there are 70% instructions are LD/ST. Assumed that unified cache has 1-port only. The hit time is 1 cycle and miss penalty is 50 cycles



Separated cache or unified cache?

Size	I-Cache	D-Cache	U-Cache
8KB	8.16	44.0	63.0
16KB	3.82	40.9	51.0
32KB	1.36	38.4	43.3
64KB	0.61	36.9	39.4
128KB	0.30	35.3	36.2
256KB	0.02	32.6	32.9

Misses per 1000 instructions

